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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/572,340	11/14/2006	Antti Iihola	SEPP0-P005	7484
27268 7590 10/09/2007 BAKER & DANIELS LLP 300 NORTH MERIDIAN STREET SUITE 2700 INDIANAPOLIS, IN 46204			EXAMINER KHOSRAVIANI, ARMAN	
			ART UNIT 2818	PAPER NUMBER
			MAIL DATE 10/09/2007	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/572,340

Applicant(s)

IIHOLA ET AL.

Examiner

Arman Khosraviani

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 17 March 2006.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-7 and 10-19 is/are pending in the application.
- 4a) Of the above claim(s) 3-7 and 13 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-2, 10-12 and 14-19 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☒ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date 05/07, 03/06.
- ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- ☐ Notice of Informal Patent Application
- ☐ Other: _____

DETAILED ACTION

1. This application contains claims directed to more than one species of the generic invention. These species are deemed to lack unity of invention because they are not so linked as to form a single general inventive concept under PCT Rule 13.1.

The species are as follows:

- I. Figures 1 through 17
- II. Figures 18 through 27
- III. Figures 28 through 29
- IV. Figures 30 through 31

Applicant is required, in reply to this action, to elect a single species to which the claims shall be restricted if no generic claim is finally held to be allowable. The reply must also identify the claims readable on the elected species, including any claims subsequently added. An argument that a claim is allowable or that all claims are generic is considered non-responsive unless accompanied by an election.

Upon the allowance of a generic claim, applicant will be entitled to consideration of claims to additional species which are written in dependent form or otherwise include all the limitations of an allowed generic claim as provided by 37 CFR 1.141. If claims are added after the election, applicant must indicate which are readable upon the elected species. MPEP § 809.02(a).

2. The claims are deemed to correspond to the species listed above in the following manner:

Claims 1-2, 10-12 and 14-19 correspond to species I

Claims 3-4 correspond to species II

Claims 5-7 correspond to species III

Claim 13 corresponds to species IV

The following claim(s) were canceled: 8 and 9.

The following claim(s) are generic: 1 and 15.

3. The species listed above do not relate to a single general inventive concept under PCT Rule 13.1 because, under PCT Rule 13.2, the species lack the same or corresponding special technical features for the following reasons: Claims 3-4 do not recite species I; as shown in Figure 11 is electrically connecting the chip 6 to the conductive layer 14 by drilling into the adhesive 5 and conductive 14 layers to form a through-hole 17, rather Claims 3-4, show chip 6 placed and connected to the conductive layer without adhesive glue 5, and the conductive layer 14 is patterned so that the pattern matches the protrusions of chip 6 while the filler 8 remains intact. Claims 5-7 do not recite species I, a second insulating-material sheet 11 is bonded to a first insulating layer 1, however the first surface consists of resin 11 and the second surface consists of the insulating material 1, not an equivalent structure as found in species I and the

disclosure does not point to how they are or can be made equivalent, Figures 28-29 and the disclosure suggest that only one surface can hold a chip 6. Claim 13 does not recite species I, the insulating layers 1, 11, 1 are not found in species I, and the conductive regions 19 form a structurally different device than species I.

4. During a telephone conversation with Mr. Kevin Erdman on September 11, 2007 a provisional election was made without traverse to prosecute the invention of I, Figures 1-17. Applicant stated Figures 1-17 correspond to claims 1-19. However, Examiner has found that invention I, corresponding to Figures 1-17, find support only in claims 1-2, 10-12 and 14-19. Note, the specification (figs. 28-31, see also pg. 19/II. 5 through pg. 20/II. 12) discloses a second sheet 11 and second insulating material sheet 11 as found in claims 5-7 only for Figures 28-31, and similarly a second sheet 11 as found in claim 13 is not found in Figures 1-17. Invention I differs structurally from claims 3 and 4; claims 3 and 4 show chip 6 placed and connected to the conductive layer without adhesive glue 5, the conductive layer 14 is patterned so that the pattern matches the protrusions of chip 6 and as a result of no through-holes, the filler 8 remains intact. Therefore, claims 3-7 and 13 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention. Affirmation of this election must be made by applicant in replying to this Office action.

5. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim

remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1 and 10-11, 15 and 17-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Shindo et al. (US 5,048,179).

Regarding claim 1, Shindo disclose (e.g. figs. 23-24, see also col. 6/ll. 3 to col. 7/ll. 10) a method for manufacturing an electronic module, comprising: taking a sheet 42, which has a first and a second surface, and which sheet includes an insulating-material layer (plastic) between the first and the second surface, as well as a conductive layer 58 on at least the first surface making at least one recess 46 in the sheet that extends through the second surface and the insulating-material layer as far as the conductive layer 58 on the first surface, which covers the recess from the direction of the first surface (58 of fig. 24), taking a component 50 having a contact surface with contact areas or contact protrusions, placing the component in the recess with its contact surface facing the first surface, attaching the component to the conductive layer, which covers the recess from the direction of the first surface (col. 6/lls. 31-46), by gluing with the aid of an electrically insulating adhesive 46, and forming a conductive

pattern from the conductive layer covering the recess and forming an electrical contact 58 between the component and the conductive pattern (col. 6/lls. 4-14) by making feed-throughs 54, 56 (contact holes), which connect at least some of the contact areas or contact protrusions of the component electrically to, the conductive pattern.

Regarding claim 10, Shindo disclose (e.g. figs. 23-24, see also col. 6/lls. 38-46) the method above, wherein at least one component is attached, and electrical contact with the conductive layer is formed by bonding the contact areas (contact holes and pads) metallurgically (58 is copper) to the conductive layer (deposition of copper), either directly, or through intermediary contact protrusions.

Regarding claim 11, Shindo disclose (e.g. figs. 23-24, see also col. 6/ll. 3 to col. 7/ll. 10) the method above, wherein at least one component attached to the conductive layer is an unpacked microcircuit chip (IC chip).

Regarding claim 15, Shindo disclose (e.g. figs. 23-24, see also col. 6/ll. 3 to col. 7/ll. 10) an electronic module, comprising: a sheet 42, which has a first and a second surface, and which sheet includes an insulating-material layer (plastic) between the first and the second surface, a conductive pattern layer 58 on at least the first surface of the sheet, at least one recess 46 in the sheet that extends through the second surface and the insulating-material layer as far as the conductive layer 58 on the first surface of the sheet, a component 50 having a contact surface with contact areas or contact protrusions, the component placed in the recess with the contact surface of the component facing the first surface, an electrically insulating adhesive 46 attaching the component to the conductive pattern layer on the first surface of the sheet (col. 6/lls. 31-

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46), and feed-throughs 54, 56 (contact holes) connecting at least some of the contact areas or contact protrusions of the component electrically to the conductive pattern layer on the first surface of the sheet.

Regarding claim 17, Shindo disclose (e.g. figs. 23-24, see also col. 6/lls. 38-46) the electronic module, wherein the feed-throughs 54, 56 (contact holes) are metal (copper) and form metallurgical bonds between the contact areas or contact protrusions of the component and the conductive pattern layer.

Regarding claim 18, Shindo disclose (e.g. figs. 23-24, see also col. 6/ll. 3 to col. 7/ll. 10) the electronic module above, wherein the component is an unpacked microcircuit chip (IC chip).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in **Graham v. John Deere Co., 383 U.S. 1, 148 USPQ 459 (1966)**, that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows: (***See MPEP Ch. 2141***)

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- a. Determining the scope and contents of the prior art;
- b. Ascertaining the differences between the prior art and the claims in issue;
- c. Resolving the level of ordinary skill in the pertinent art; and
- d. Evaluating evidence of secondary considerations for indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 2, 12, 14, 16 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shindo et al. (US 5,048,179) in view of Nakamura (US 2007/0166886).

Regarding claim 2, it is noted that Shindo do not teach the method above, wherein the components are placed facing both the first and second surface in the insulating-material layer and electrical contacts are formed to the components in such a way that at least some of the components are connected to the conductive layer on the first surface and at least some to the conductive layer on the second surface.

However, Nakamura teaches (e.g. fig. 3, see also pg. 3/pps. 0037-0044) the method above, wherein the components 15 or 16 are placed facing both the first and second surface in the insulating-material layer 11 (glass) and electrical contacts 13 are formed to the components in such a way that at least some of the components are

connected to the conductive layer on the first surface and at least some to the conductive layer on the second surface (pg. 3/pp. 0040).

Since the combination of Shindo and Nakamura teach the method above, it would have been obvious to a have the components placed facing both the first and second surface in the insulating-material layer and electrical contacts formed to the components in such a way that at least some of the components are connected to the conductive layer on the first surface and at least some to the conductive layer on the second surface of Nakamura in Shindo for the benefit of providing a simple and reliable method of manufacturing electronic modules containing embedded components.

Regarding claim 12, it is noted that Shindo do not explicitly teach the method above, wherein, in order to create a multi-layer circuit-board structure, additional insulating layers and conductive layers are manufactured on the first and/or the second surface.

However, Nakamura teaches (e.g. fig. 3, see also pg. 3/pp. 0037-0044) the method above, wherein, in order to create a multi-layer circuit-board structure (e.g. fig. 3), additional insulating layers 11 and conductive layers 13 are manufactured on the first and/or the second surface.

Since the combination of Shindo and Nakamura teach the method above, it would have been obvious to a have the method wherein, in order to create a multi-layer circuit-board structure, additional insulating layers and conductive layers are manufactured on the first and/or the second surface of Nakamura in Shindo for the

benefit of providing a simple and reliable method of manufacturing electronic modules containing embedded components.

Regarding claim 14, it is noted that Shindo do not explicitly teach the method above, wherein a conductive-pattern layer is manufactured on both the first and the second surfaces of the insulating-material layer.

However, Nakamura teaches (e.g. fig. 3, see also pg. 3/pp. 0037-0044) the method above, wherein a conductive-pattern layer 13 is manufactured on both the first and the second surfaces of the insulating-material layer 11.

Since the combination of Shindo and Nakamura teach the method above, it would have been obvious to have the conductive-pattern layer manufactured on both the first and the second surfaces of the insulating-material layer of Nakamura in Shindo for the benefit of providing a simple and reliable method of manufacturing electronic modules containing embedded components.

Regarding claim 16, it is noted that Shindo do not teach the electronic module above, comprising: a second conductive pattern layer on the second surface of the sheet, a second component placed in the insulating-material layer and facing the second conductive pattern layer, and electrical contacts connecting the second component to the second conductive pattern layer.

However, Nakamura teaches (e.g. fig. 3, see also pg. 3/pp. 0037-0044) comprising: a second conductive pattern layer 13 on the second surface of the sheet 11, a second component 15 placed in the insulating-material layer and facing the

second conductive pattern layer, and electrical contacts 13 connecting the second component to the second conductive pattern layer (pg. 3/pp. 0040).

Since the combination of Shindo and Nakamura teach the method above, it would have been obvious to a second conductive pattern layer on the second surface of the sheet, a second component placed in the insulating-material layer and facing the second conductive pattern layer, and electrical contacts connecting the second component to the second conductive pattern layer of Nakamura in Shindo for the benefit of providing a simple and reliable method of manufacturing electronic modules containing embedded components.

Regarding claim 19, it is noted that Shindo do not explicitly teach the electronic module above, comprising a further insulating layer and a further conductive layer on the first surface of the sheet.

However, Nakamura teaches (e.g. fig. 3, see also pg. 3/pp. 0037-0044) the electronic module above, comprising (e.g. fig. 3) a further insulating layer 11 and a further conductive layer 13 on the first surface of the sheet.

Since the combination of Shindo and Nakamura teach the method above, it would have been obvious to a have a further insulating layer and a further conductive layer on the first surface of the sheet of Nakamura in Shindo for the benefit of providing a simple and reliable method of manufacturing electronic modules containing embedded components.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Boucquet (US 5,042,145), Adachi et al. (US 5,081,562), Leedy (US 5,654,220), Leedy (US 5,840,593), Leedy (US 5,985,693), Kinsman (US 2003/0068877), Kinsman (US 2003/0067074), Oya (US 2004/0000710), and Kimura et al. (US 6,806,428) show methods similar to the instant invention.

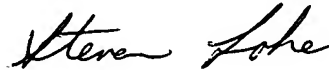
6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Arman Khosraviani whose telephone number is 571-272-2554. The examiner can normally be reached on Monday to Friday, 7:30a - 5:00p (Eastern Time).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven Loke can be reached on 571-272-1657. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AK

STEVEN LOKE
SUPERVISORY PATENT EXAMINER

A handwritten signature in black ink, appearing to read "Steven Loke", is positioned below the printed name and title.